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1 Feature Summary

- all signals on SH1WH expansion bus broken out into 0.1" spaced dual-row header pads
- $V_{\text{util}}$ regulator (+5V linear regulator)
- Optional FPGA for 32 lines of enhanced digital I/O

![Block Diagram of SH1WH Breakout-Board]

Figure 1: Block Diagram of SH1WH Breakout-Board
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Descriptive Specifications

1.1 Power Supply
The SH1WH-BB1 has a screw-type terminal block for connecting power to both the breakout board and other boards in the expansion connector stack. The voltage applied to the terminal block is distributed to other boards in two forms; the raw voltage is applied to other boards as $V_{batt}$, and a regulated +5V voltage is provided as $V_{util}$. The voltage input is restricted to a range of 6.8V to 13V due to the +5V linear regulator on board the breakout board (the SH1WH alone can accept voltages as low as 3.8V by itself). The +5V regulated output is used by the FPGA. Boards without the FPGA option that do not use $V_{util}$ can operate at lower voltages without failure.

1.2 Jumper Locations and Pinouts
The SH1WH-BB1 has 8 headers and one terminal block total. The headers are provided unpopulated so the user can put either male or female connectors of various lengths and styles, depending on the user's application.

1.2.1 JP1 – Analog Header
The analog header breaks out 8 A/D channels as well as 2 D/A channels and their reference voltages. Note that the grounds on this header are the analog grounds, and they should not be tied to the digital grounds for best analog performance. The tie point between analog and digital grounds is internal to the SH1WH board.

Figure 2: Analog header pinouts (all views from top)

1.2.2 JP2 – Power Management and SH-1 Direct I/O
The power management and SH-1 Direct I/O header breaks out both $V_{batt}$ and $V_{util}$ voltages, along with all the power management signals (RESET, NMI, shutdown, and wake up). Also provided on this header are the five A-port processor direct signals; the exact function of these signals is configurable inside the SH-1. Note that these A-port processor direct signals are used to program the FPGA, and thus if the FPGA option is populated, these signals become unavailable for general use.
1.2.3 JP3 – A/D Trigger Header

The A/D trigger header is provided so users can connect an external A/D trigger source to the SH1WH for precise timing of A/D sampling. Note that this header has DGND (not AGND) as a reference, since the trigger signal is a digital signal. Also note that the A/D trigger feature can not be used at the same time with multiplexed address/data peripherals on the processor expansion header, as the address hold (AH) function is also multiplexed on to this pin inside the SH-1.

AH/samp 1 2 DGND

Figure 4: A/D Trigger Header Pinouts

1.2.4 JP5 – Motor Control Header

All motor control lines are made available on this header for diagnostic purposes. This also allows for a configuration of breakout-board plus motor driver card in case users already have a PWM signal source that they want to connect to the motor driver card.

DGND 1 2 DGND
PWM0 3 4 PWM1
EN0 5 6 EN1
DIR0 7 8 DIR1
DGND 9 10 DGND
PWM2 11 12 PWM3
EN2 13 14 EN3
DIR2 15 16 DIR3
PWM4 17 18 DIR4
EN4 19 20 DGND

Figure 5: Motor Control Header Pinouts

1.2.5 JP6 – Processor Expansion Header

The processor expansion header allows users to connect extra memory-mapped peripherals to the SH-1.
### 1.2.6 JP7 – Vutil Breakout Header

The Vutil breakout header is provided so users can have a convenient source of regulated +5V for their projects. There are a couple of NC pins so users can put in a keyed connector to prevent users from plugging in a power connector backwards.

<table>
<thead>
<tr>
<th>Vutil 1</th>
<th>Vutil 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC 3</td>
<td></td>
</tr>
<tr>
<td>PGND 4</td>
<td>NC 5</td>
</tr>
<tr>
<td>PGND 6</td>
<td></td>
</tr>
</tbody>
</table>

#### Figure 7: Vutil breakout header

### 1.2.7 JP8 – Vbatt Breakout Header

The Vbatt breakout header is provided so users can have a convenient source of unregulated power. It also provides an alternative method to connecting up Vbatt if they do not wish to use the terminal block.

<table>
<thead>
<tr>
<th>Vbatt 1</th>
<th>Vbatt 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC 3</td>
<td></td>
</tr>
<tr>
<td>PGND 4</td>
<td>NC 5</td>
</tr>
<tr>
<td>PGND 6</td>
<td></td>
</tr>
</tbody>
</table>

#### Figure 8: Vbatt breakout header
1.2.8 JP9 – Enhanced Digital I/O Header

The enhanced digital I/O header breaks out 32 signals plus ground from the FPGA. These signals can take on a large number of functions, depending on what configuration the FPGA has.

<table>
<thead>
<tr>
<th>PIN</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DGND</td>
</tr>
<tr>
<td>2</td>
<td>DGND</td>
</tr>
<tr>
<td>3</td>
<td>DIG0</td>
</tr>
<tr>
<td>4</td>
<td>DIG1</td>
</tr>
<tr>
<td>5</td>
<td>DIG2</td>
</tr>
<tr>
<td>6</td>
<td>DIG3</td>
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<tr>
<td>7</td>
<td>DIG4</td>
</tr>
<tr>
<td>8</td>
<td>DIG5</td>
</tr>
<tr>
<td>9</td>
<td>DIG6</td>
</tr>
<tr>
<td>10</td>
<td>DIG7</td>
</tr>
<tr>
<td>11</td>
<td>DGND</td>
</tr>
<tr>
<td>12</td>
<td>DGND</td>
</tr>
<tr>
<td>13</td>
<td>DIG8</td>
</tr>
<tr>
<td>14</td>
<td>DIG9</td>
</tr>
<tr>
<td>15</td>
<td>DIG10</td>
</tr>
<tr>
<td>16</td>
<td>DIG11</td>
</tr>
<tr>
<td>17</td>
<td>DIG12</td>
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<td>DIG15</td>
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<tr>
<td>21</td>
<td>DGND</td>
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<td>22</td>
<td>DGND</td>
</tr>
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<td>23</td>
<td>DIG16</td>
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<td>DIG22</td>
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<tr>
<td>30</td>
<td>DIG23</td>
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<td>31</td>
<td>DGND</td>
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<td>32</td>
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<td>DIG27</td>
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<td>DIG28</td>
</tr>
<tr>
<td>38</td>
<td>DIG29</td>
</tr>
<tr>
<td>39</td>
<td>DIG30</td>
</tr>
<tr>
<td>40</td>
<td>DIG31</td>
</tr>
</tbody>
</table>

Figure 9: Enhanced Digital I/O Header Pinouts

1.2.9 V\textsubscript{batt} Terminal Block

The V\textsubscript{batt} terminal block provides convenient screw terminals to which users can connect voltages from 6.8V to 13V to power the card stack.

Figure 10: Terminal Block Pinouts
1.3 Signal Descriptions

1.3.1 Direct Processor Bus Signals

**AD[7:0] I/O**  Multimode address and data bus. Depending on access location, this bus may behave either as a multiplexed address/data bus or as just a data bus. This bus may also be treated as either a simple 8-bit bus or the lower byte of a 16-bit wide bus.

**A[7:0] O**  Address bits from the processor

**RD O**  Read enable from the processor, active low

**WR O**  Write enable from the processor, active low

**CS7 O**  Chip select from the processor, active low. This CS line corresponds to 8-bit accesses with an unmultiplexed bus mode in addresses from 0x7000000 to 0x7FFFFFF.

**CS6 O**  Chip select from the processor, active low. This CS line corresponds to 8 or 16-bit wide accesses in a multiplexed address/data bus mode in addresses from 0x6000000 to 0x6FFFFFF; if the 14th address bit is high, then the bus behaves as if it were 16 bits wide; if it is low, then the bus behaves as if it were 8 bits wide. It also corresponds to 16-bit accesses in an unmultiplexed bus mode in addresses from 0xE000000 to 0xEFFFFFF.

**RES I/O**  Hard reset, active low. This signal is debounced and pulled low for 250 ms on any of the following conditions: reset button depressed, Vcc out of range (2.88V typ.), power-on reset, or watchdog timer time-out (if enabled). A hard reset will clear processor state and is required to wake up out of deep-sleep modes. RES is a wired-AND signal, so users may pull RES low to force a reset condition.

**CLK O**  12 MHz clock signal, synchronous to direct processor bus signals

**NMI O**  Non-maskable interrupt output. This signal is triggered when the alarm clock in the RTC times out, or when the user depresses the NMI button.

**AH/samp I/O**  Software configurable pin to either address hold output or A/D sample trigger input. Address hold is used when the expansion bus is in multiplexed address/data mode. A/D sample trigger is optional as the sample trigger can be set by software as well.
1.3.2 Digital I/O

PA[15:11]  I/O Programmable function digital I/O ports. In addition to simple digital I/O, PA[15:12] can also be remapped in software to function as active-low interrupt lines or DMA handshaking lines; PA11 can be remapped to function as a timing pattern generator output.

PWM[4:0]  I/O Pulse width modulation control output. Dedicated hardware drive these lines with square waves of varying duty cycles; properties of the PWM output are set by software. These signals can also be configured to function as digital I/O, timing pattern generator outputs, or as interval timer inputs.

EN[4:0]  O Dedicated digital outputs. While the label may suggest that it can be used to enable motors under PWM control, this output may be used for any function. EN[4:0] maps to bits 4:0 of any data written to locations ranging from 0xA000000 through 0xAFFFFFF.

DIR[4:0]  O Dedicated digital outputs. While the label may suggest that it can be used to set the direction of motors under PWM control, this output may be used for any function. DIR[4:0] maps to bits 12:8 of any data written to locations ranging from 0xA000000 through 0xAFFFFFF.

1.3.3 Analog Signals

AN[7:0]  I Input to A/D converter. The A/D converter is a 10-bit SAR type converter.

Aout[1:0]  O Output of D/A converters. The D/A converters have 12-bit resolution.

AVrefI  O Reference voltage used by the A/D converter. This AGND-referenced voltage represents the maximum voltage that the A/D converter can sample. Excessive current draw from this output will affect A/D converter accuracy.

AVrefO  O Reference voltage used by the D/A converter. This AGND-referenced voltage represents the maximum voltage output by the D/A converter. Excessive current draw from this output will affect D/A converter accuracy.

AGND  PWR Analog ground. This is an isolated, low-current return path for analog signals.
1.3.4 Power Control

**shutdwn**  
A high input on this pin causes the switching regulator to shut down, effectively turning the board off. This input is internally tied low with a 10K resistor.

**wakeout**  
This is an alarm clock output that functions regardless of the state of Vcc. Its polarity and trigger time is programmable. It is internally connected to the NMI of the processor.

1.3.5 Power

**Vutil**  
This is a utility voltage pin provided on the expansion headers for use by expansion cards. It is not connected on the SH1WH.

**DGND**  
Digital signal ground.

**PGND**  
Power ground; high current return path for system power.

**Vbatt**  
System power. Nominally provided by a battery, but any unregulated DC input between 3.8 and 13V is acceptable.

1.3.6 Miscellaneous

**NC**  
Internally not connected. For use by expansion cards.

2 Location of Headers

![Location of headers and respective pin 1 locations](image)

Figure 11: Location of headers and respective pin 1 locations
3 UCF-Format Pin Locations for FPGA

The following listing is a Xilinx User Constraint File (.UCF) compatible mapping of pin numbers to pin functions for the FPGA aboard the SH1WH-BB1-FPGA. This listing assumes the user places all I/O functions into a hierarchical block with the designator "U1". This listing is compatible with the Xilinx Foundation Series tools, version 1.5. An archived sample project with this information in a .UCF file for the Xilinx tools is available on the web at http://www.ai.mit.edu/people/bunnie/sh1wh/fpga.zip.

```
NET U1/PCLK   LOC = P2;
NET U1/DIG0   LOC = P3;
NET U1/DIG1   LOC = P7;
NET U1/DIG2   LOC = P8;
NET U1/DIG3   LOC = P9;
NET U1/DIG4   LOC = P10;
NET U1/DIG5   LOC = P13;
NET U1/DIG6   LOC = P14;
NET U1/DIG7   LOC = P15;
NET U1/DIG8   LOC = P16;
NET U1/DIG9   LOC = P17;
NET U1/DIG10  LOC = P18;
NET U1/DIG11  LOC = P19;
NET U1/DIG12  LOC = P20;
NET U1/HDC    LOC = P28;
NET U1/DIG13  LOC = P29;
NET U1/DIG14  LOC = P31;
NET U1/DIG15  LOC = P32;
NET U1/DIG16  LOC = P33;
NET U1/DIG17  LOC = P34;
NET U1/DIG18  LOC = P35;
#NET U1/P_PA14 LOC = P36;
NET U1/DIG19  LOC = P39;
NET U1/DIG20  LOC = P40;
NET U1/DIG21  LOC = P41;
NET U1/DIG22  LOC = P42;
NET U1/DIG23  LOC = P43;
NET U1/DIG24  LOC = P44;
NET U1/DIG25  LOC = P45;
NET U1/DIG26  LOC = P46;
NET U1/DIG27  LOC = P47;
#NET U1/P_PA15 LOC = P50;
#NET U1/P_PA13 LOC = P52;
NET U1/P_PA13C1 LOC = P58;
NET U1/P_PA13C2 LOC = P54;
NET U1/DIG28  LOC = P53;
NET U1/DIG29  LOC = P55;
NET U1/DIG30  LOC = P56;
NET U1/DIG31  LOC = P57;
NET U1/P_TIOCA4 LOC = P59;
```
NET U1/P_AD5   LOC = P67;
NET U1/P_AD6   LOC = P68;
NET U1/P_AD7   LOC = P69;
NET U1/P_A0   LOC = P70;
NET U1/P_A1   LOC = P71;
#NET U1/P_PA12   LOC = P72;
#NET U1/P_PA11   LOC = P74;
NET U1/P_A2   LOC = P78;
NET U1/P_A3   LOC = P80;
NET U1/P_A4   LOC = P81;
NET U1/P_A5   LOC = P82;
NET U1/P_A6   LOC = P83;
NET U1/P_A7   LOC = P84;
NET U1/P_AH_N   LOC = P85;
NET U1/P_CS6_N   LOC = P86;
NET U1/P_CS7_N   LOC = P87;
NET U1/P_RD_N   LOC = P90;
NET U1/P_WR_N   LOC = P91;
NET U1/RESET   LOC = P92;
NET U1/SHUTDOWN   LOC = P93;
NET U1/NMI   LOC = P94;
NET U1/WD_TRIG   LOC = P95;
NET U1/P_TIOCA0   LOC = P96;
NET U1/P_TIOCA1   LOC = P97;
NET U1/P_TIOCA2   LOC = P98;
NET U1/P_TIOCA3   LOC = P99;